

 <div data-bbox="491 98 539 264" style="display: inline-block; vertical-align: middle;"> I Q R </div>	IBIS QUALITY REPORT	date	1 (8)
		5-Apr-13	

IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	m24c32_mlp2x3.ibs
IBIS Version:	4.0

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1. MODELING

IBIS (I/O, Buffer, Information, Specification) models provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, of representing the electrical characteristics of digital IC's pins behaviourally

1.1 Component description

Component name	Technology	Component description
M24C32 (32 Kb) M24C64 (64 Kb) M24128 (128 Kb) M24256 (256 Kb) M24512 (512 Kb) M24M01 (1 Mb) M24M02 (2 Mb)	CMOS F8H/P2	The M24xxx are EEPROM devices accessed through a serial I ² C-bus memory. These devices are qualified to operate from -40°C to +85°C, over a supply voltage range of 1.8V / 5.5V. The M24xxx IBIS model is the same for each M24xxx device from 32Kb up to 1Mb.

1.2 Modeling conditions

Simulator used	AMS 2010.1 (Mentor Graphics)
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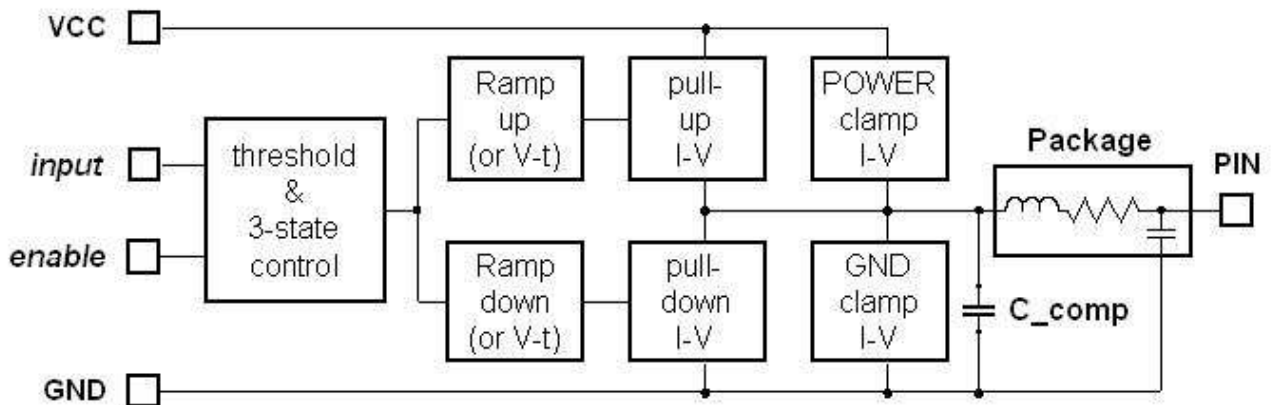


Figure 1 – IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	125
Voltage Supply * [Volt]	3.00	1.80	5.50
Process setting	nom	weak	strong

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* Different Voltage Reference (only if Voltage Supply is not present)	Typical	Minimum	Maximum
Pullup Voltage Reference [Volt]	-	-	-
Pulldown Voltage Reference [Volt]	-	-	-
Power Clamp Voltage Reference [Volt]	-	-	-
GND Clamp Voltage Reference [Volt]	-	-	-

Model names (of Component)	Model Type	C_comp (typ, min, max)
mod_en	Input	2.219pF (typ), 2.024pF (min) , 2.433pF (max)
mod_sda	I/O_Open_Drain	2.925pF (typ), 2.793pF(min) , 3.207pF (max)
mod_scl	Input	2.219pF (typ), 2.024pF (min) , 2.433pF (max)
mod_wcn	Input	2.219pF (typ), 2.024pF (min) , 2.433pF (max)

Model names (of Component)	Threshold and Vmeas	Timing parameters (if used)
mod_in	Vinl=0.90V , Vih=2.10V	
mod_out	Vmeas=1.50V	Rref=1k, Cref=10pF, Vref=3.0V

Package	description/comment
MLP 2x3	8 lead micro leadframe outline

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1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.

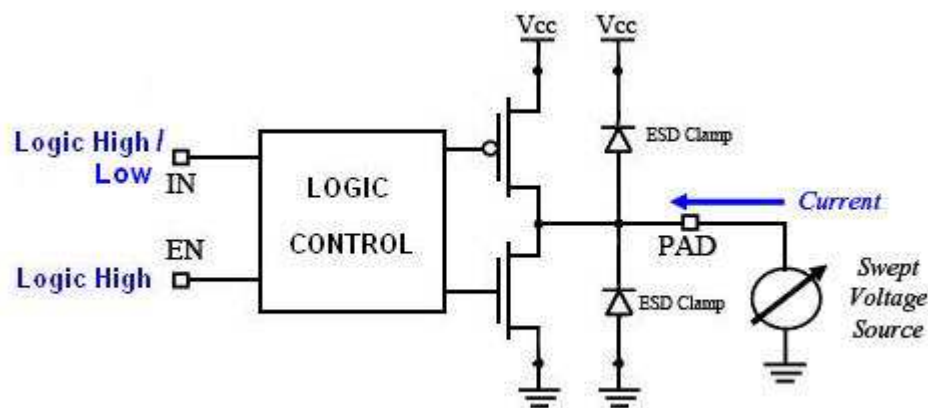


Figure 2 – Simulation Setup to extract I/V data from I/O model type

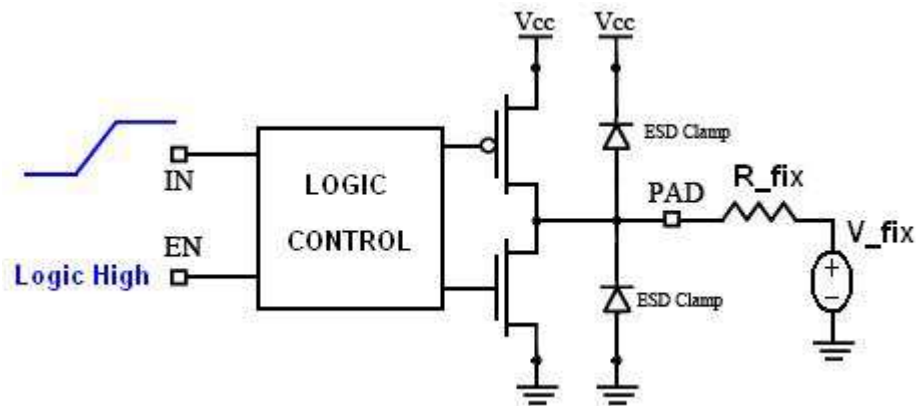


FIGURE 3 – SIMULATION SETUP TO EXTRACT V/T DATA FROM I/O MODEL TYPE
Extracting V/T conditions:

V-T data condition extractions	Load conditions	Adding conditions
Rising waveform	R_fix=50 Ohm, V_fix= 0 V	
Rising waveform	R_fix=50 Ohm, V_fix= 3.0 V	
Falling waveform	R_fix=50 Ohm, V_fix= 3.0 V	
Falling waveform	R_fix=50 Ohm, V_fix= 0 V	

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2. IBISCHK5 CHECK

The created IBIS model must be checked using IBISCHK5 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

2.1 Result Check by IBISCHK5

IBISCHK5 V5.0.4

Checking m24c32_mlp2x3.ibs for IBIS 4.2 Compatibility...

NOTE (line 282) - Pulldown Maximum data is non-monotonic

NOTE (line 285) - Pulldown Typical data is non-monotonic

NOTE (line 286) - Pulldown Minimum data is non-monotonic

WARNING - Combined Pulldown for Model: mod_sda Typical data is non-monotonic

Errors : 0

Warnings: 1

File Passed

Adding comments about the Warning or Note:
<p>The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.</p>

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3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions (figure 4), must be matched. These output comparisons are presented in TYP, MIN and MAX condition. This section can't be defined for Input and Terminator model type, because they are input-only model types.

How well results are matched?	Put "X" into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshot and/or Undershot regions.	
Curves match well.	X

3.1 Functional verification:

Circuit used for output comparison results is illustrated in figure 4.

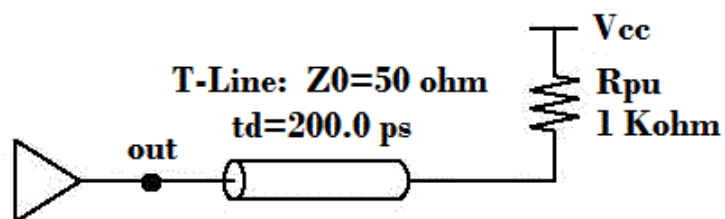


Figure 4 – Circuit used for Functional Check

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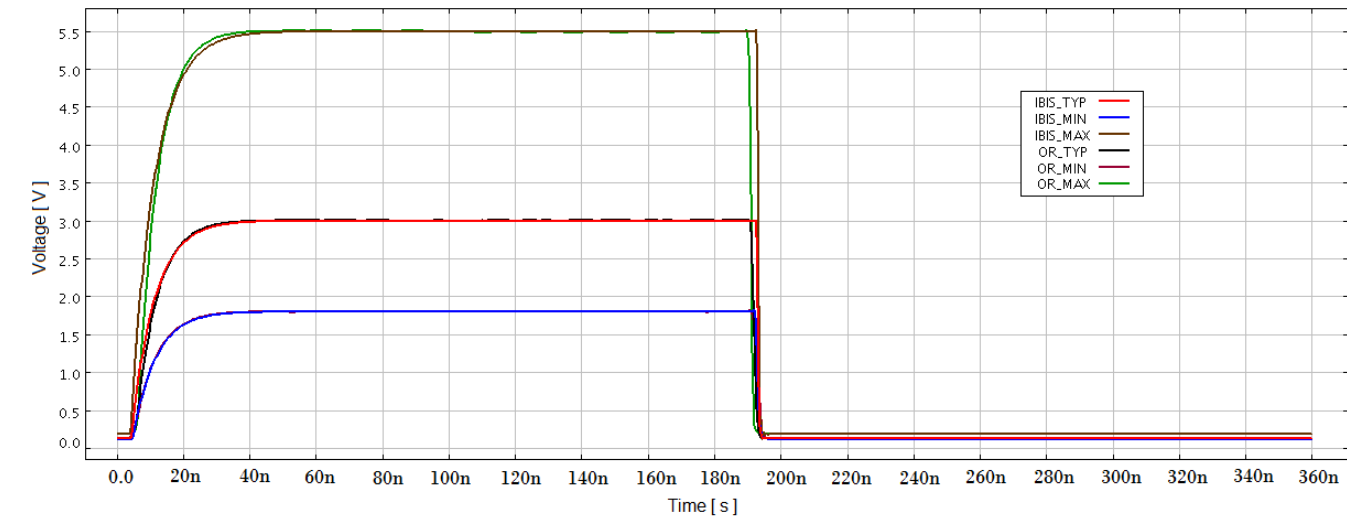


Figure 5 – IBIS vs Eldo comparison results of “mod_sda” Model

Output Comparisons:

Adding comments about the comparison:

4. EXTRA INFORMATION

This section can contains other extra informations, to explain some other features of peculiar IBIS model

Other specifications	description